Code No: 126EN **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech III Year II Semester Examinations, May - 2016
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Define g_m of MOS transistor. [2]
b) Draw transfer characteristics of CMOS inverter. [3]
c) Define scaling and explain it. [2]
d) Explain difference between stick diagram and layout diagram. [3]
e) Define delay and explain different time delays in gate level modeling. [2]
f) Explain the importance of wiring capacitance of a MOS transistor. [3]
g) Explain the difference between EPROM and EEPROM. [2]
h) Draw 2-bit comparator. [3]
i) Explain difference between PLA and PAL. [2]
j) Define controllability and observability with respect to testing. [3]

PART - B

(50 Marks)

2. Draw the fabrication steps of CMOS transistor and explain its operation in detail. [10]

OR

3. Draw the fabrication steps of NMOS transistor and explain its operation in detail. [10]

4.a) Draw the flow chart of VLSI Design flow and explain the operation of each step in detail.
b) Draw the stick diagram for three input AND gate. [6+4]

OR

5. What is the purpose of design rule? What is the purpose of stick diagram? What are the different approaches for describing the design rule? Give three approaches for making contacts between poly silicon and discussion in NMOS circuit. [10]

6.a) Draw and explain fan in and fan out characteristics of different CMOS design technologies.
b) Explain different wiring capacitance used in Gate level design with example. [5+5]

OR

7. What are the alternate gate circuits available? Explain any one of item with suitable sketch by taking NAND gate as an example. [10]

8.a) Draw the basic circuit diagram of static RAM and explain its operation.
b) Draw the basic block diagram of 4-bit adder and explain its operation in detail. [5+5]

OR

9.a) Explain the CMOS system design based on the I/O cells with suitable example.
b) Design a four bit parity generator using only XOR gates and draw the Schematic of it. [5+5]

10.a) Why the chip testing is needed? At what levels testing a chip can occur?
b) What is the drawback of serial scan? How to overcome this? [5+5]

OR

11.a) Briefly Explain different parameters influencing low power design in detail.
b) What is sequential fault grading? Explain how it is analyzed. [5+5]

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Code No: 126EN **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year II Semester Examinations, October/November - 2016
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	Define threshold voltage of a MOS device.	[2]
b)	What are pull-ups and write about the resistor pull-up and its usage.	[3]
c)	Explain about the contact cuts and approaches.	[2]
d)	Represent the Stick diagram of a NMOS inverter.	[3]
e)	Write about the clocked CMOS logic and its usage.	[2]
f)	Explain about the Wiring capacitance and its need.	[3]
g)	Mention about SRAM and its usage.	[2]
h)	Describe about the Serial Access Memories.	[3]
i)	Explain about the principle of Built in Self Test.	[2]
j)	Explain about test Principles used for testing.	[3]

PART - B

(50 Marks)

2.a) Write about BiCMOS fabrication in a n-well process with a diagram.
b) Distinguish between Bipolar and CMOS devices technologies in brief. [5+5]

OR

3.a) Mention about the BICMOS Inverters and alternative BICMOS Inverters.
b) Determine the pull-up to pull down ratio for NMOS inverter driven by another NMOS Inverter. [5+5]

4.a) Discuss about the stick diagrams and their corresponding mask layout examples.
b) Draw the stick diagram of p-well CMOS inverter and explain the process. [5+5]

OR

5.a) Explain about the 2 μm CMOS Design rules and discuss with a layout example.
b) Draw and explain the layout for CMOS 2-input NAND gate. [5+5]

6. Discuss about the logics implemented in gate level design and explain the switch logic implementation for a four way multiplexer. [10]

OR

7.a) Describe about the methods for driving large capacitive loads.
b) Describe about the choice of fan – in and fan – out selection in gate level design. [5+5]

8.a) Design a shift register with the dynamic latch operated by a two-phase clock.
b) Explain the working principle of Ripple carry adder using Transmission Gates. [5+5]

OR

9.a) Explain about the Wallace tree multiplication and its design issues.
b) Draw the circuit diagram of four transistor DRAM cell with storage nodes. [5+5]

10.a) Explain the detailed logic configurable Block Architecture of FPGA.
b) Write a note on the different Parameters influencing low power design. [5+5]

OR

11. Explain the following in detail.
a) Chip level Test Techniques
b) Testability and practices. [5+5]

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Code No: 126EN **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year II Semester Examinations, May - 2017
VLSI DESIGN
(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	What are the advantages of BiCMOS process compare with the CMOS.	[2]
b)	List the fabrication procedures for IC Technologies.	[3]
c)	Draw the VLSI Design Flow.	[2]
d)	Draw the stick diagram for two inputs NOR gate.	[3]
e)	What is switch logic?	[2]
f)	What are the issues involved in driving large capacitive loads in VLSI circuits.	[3]
g)	Design a 2-bit Parity generator.	[2]
h)	What is Booth's algorithm?	[3]
i)	Write the Comparison between FPGA and CPLD.	[2]
j)	What type of faults can be reduced by improving layout design?	[3]

PART - B

(50 Marks)

2.a) Discuss the Basic Electrical Properties of MOS and BiCMOS Circuits.
b) Derive the expression for estimation of Pull-Up to Pull-Down ratio of an n-MOS inverter driven by another n-MOS inverter. [5+5]

OR

3.a) Derive the relationship between I_{ds} and V_{ds}
b) Derive the expression for transfer characteristics of CMOS Inverter. [5+5]

4.a) Explain in detail about the scaling concept in VLSI circuit Design.
b) Draw the Layout Diagrams for NAND Gate using nMOS. [5+5]

OR

5.a) Explain λ-based Design Rules in VLSI circuit Design.
b) Draw the Layout Diagrams for CMOS Inverter. [5+5]

6. Explain the following:
a) Fan-in
b) Fan-out
c) Choice of layers. [10]

OR

7. Describe the following:
a) Pseudo-nMOS Logic
b) Domino Logic. [5+5]

8.a) Draw the schematic and logic diagram for a single bit adder and explain its operation with truth table.

b) With neat circuit diagram, explain the operation of Barrel shifter. [5+5]

OR

9.a) Explain about Serial access memories.

b) Explain about design of an ALU subsystem in brief. [5+5]

10.a) Explain Architecture of FPGA in detail.

b) What are the draw backs of PLAs? How PLAs are used to implement combinational and sequential logic circuits? [5+5]

OR

11.a) Why stuck-at faults occur in CMOS circuits? Explain with suitable logical diagram.

b) Why the chip testing is needed? At what levels testing a chip can occur? [5+5]

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Code No: 126EN **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year II Semester Examinations, December - 2017
VLSI DESIGN
(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART – A

(25 Marks)

1.a)	What is pull up and pull down device?	[2]
b)	Why NMOS technology is preferred more than PMOS technology?	[3]
c)	What are the uses of Stick diagram?	[2]
d)	What is the fundamental goal in Device modeling?	[3]
e)	List out the sources of static and dynamic power consumption.	[2]
f)	Define Fan-in and Fan-out.	[3]
g)	Why is barrel shifter very useful in the designing of arithmetic circuits?	[2]
h)	Write the principle of any one fast multiplier.	[3]
i)	What is programmable logic array?	[2]
j)	What are feed-through cells? State their uses.	[3]

PART – B

(50 Marks)

2.a)	What is meant by latch up problem? How will you prevent.	
b)	Define threshold voltage? Drive the Vt equation for MOS transistor.	[5+5]
	OR	
3.a)	Explain with neat diagrams the various NMOS fabrication technology.	
b)	Draw and explain BiCMOS inverter circuit.	[5+5]
4.	Draw the circuit diagram, stick diagram and layout for CMOS inverter.	[10]
	OR	
5.a)	Explain about the various layout design rules.	
b)	Draw the static CMOS logic circuit for the following expression i) $Y=(ABCD)'$ ii) $Y=[D(A+BC)]'$	[5+5]
6.a)	Explain different capacitances present in CMOS design.	
b)	Explain the concept of MOSFET as switches with suitable example.	[5+5]
	OR	
7.	Write short notes on: a) Ratioed Circuits b) Dynamic Circuits.	[5+5]

8.a) Explain the operation of a basic 4 bit adder.
b) Explain the operation of booth multiplication with suitable example. [5+5]

OR

9.a) Design a 1:16 demultiplexer using 1:8 demultiplexers.
b) Draw the structure of a 4×4 static RAM and explain it's operation. [5+5]

10.a) Discuss any two types of programming technology used in FPGA design.
b) Explain ATPG fault models. [5+5]

OR

11.a) What is programmable devices? How it differs from ROM?
b) Explain fault models of VLSI Design. [5+5]

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Code No: 126VN **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, April - 2018

VLSI DESIGN

(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	Define figure of merit of MOS transistor.	[2]
b)	Draw the CMOS inverter circuit.	[3]
c)	What is meant by synthesis?	[2]
d)	Differentiate Functional simulation and timing simulation.	[3]
e)	What is the importance of fan-in and fan-out?	[2]
f)	Differentiate rise time and fall time.	[3]
g)	Draw the 1-bit SRAM cell.	[2]
h)	What are the various serial access memories?	[3]
i)	Implement 2:1 MUX using PAL.	[2]
j)	What is the difference between verification and validation?	[3]

PART - B

(50 Marks)

2. Draw and explain the operation of BiCMOS inverter. [10]

OR

3. Derive the drain to source current equation for NMOS enhancement mode transistor. [10]

4. Discuss the steps involved in VLSI design flow. [10]

OR

5. Draw the stick diagram for the following Boolean expression using CMOS logic. $F = A(B + C)$. [10]

6. Briefly explain the commonly used technique to estimate the delay time of a MOS inverter. [10]

OR

7. Implement 4:1 multiplexer using switch logic. [10]

8. Design a 4-bit magnitude comparator. [10]

OR

9. Design a zero detector circuit. [10]

10. Discuss scan design Techniques. [10]

OR

11. Compare various programmable devices. [10]

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Code No: 126VN **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech III Year II Semester Examinations, December - 2018
VLSI DESIGN
(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	Write about the Pass transistor.	[2]
b)	Distinguish between Enhancement and Depletion mode transistor action in N-MOS.	[3]
c)	Write about contacts and vias in layout design.	[2]
d)	Write about the 1.2 μm double metal single poly CMOS rules.	[3]
e)	Mention the different forms of Time delays in gate level circuits.	[2]
f)	Explain about Switch logic and its usage.	[3]
g)	Distinguish a synchronous and an asynchronous counters.	[2]
h)	Write a note on Content Addressable Memory.	[3]
i)	What is the need for testing of IC?	[2]
j)	What are the different chip-level Test Techniques?	[3]

PART - B

(50 Marks)

2.a) Explain the CMOS fabrication process in p-well using suitable diagrams.
b) Discuss the effect of threshold voltage on MOSFET current Equations. [5+5]

OR

3.a) Discuss the MOS transistor Characteristics in Depletion and enhancement modes.
b) Write about Alternative forms of pull-up and describe about the NMOS pull-ups. [5+5]

4. Write about the stick diagrams and design a stick diagram for two input N-MOS NAND and NOR gates. [10]

OR

5.a) Distinguish between the Lambda-base rules and Double metal MOS process rules.
b) Draw the neat layout diagrams for NMOS shift register cell. [5+5]

6.a) Explain the formal estimation of CMOS inverter delay rise-time estimation and Fall-time estimation.
b) Write a note on the Wiring capacitance in detail. [5+5]

OR

7.a) Write about the different Alternate gate circuits in detail.
b) Discuss about the Choice of layers for the gate level design. [5+5]

8.a) Explain the working principle of Ripple carry adder using Transmission Gates.
b) Explain about the configurations and applications of SRAM and DRAM cells. [5+5]

OR

9.a) Explain the Principle and structure of Serial-Parallel multiplier.
b) Describe the design procedure for design of a asynchronous counter. [5+5]

10.a) Design a PAL to realize a full Adder circuit.
b) Explain the detailed Architecture of CPLD and its Implementations. [5+5]

OR

11. Write a short note on the following:
a) CMOS Testing
b) Strategies for testing. [5+5]

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